

Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
Phone: (800) ANALOG-D or (781) 461-3881, FAX: (781) 461-3010, EMAIL: dsp.support@analog.com

SHARC Link Port Timing Notes

Last Modified: 6/19/97

OVERVIEW:

This Engineer's Note will show how to calculate for maximum skew allowed between LCLK and LDATA at a receiver link port, as well as how to calculate the maximum transmission delay between 2 link ports.

Updated 11/11/96

Changes to the datasheet dated 4/96:

These specifications are "final" for rev. 2.0 ADSP-21062.

1x CLK Speed Operation:

$t_{LCLKTWL} \quad (t_{CK}/2)+1.25 \text{ Max}$

$t_{LCLKTWH} \quad (t_{CK}/2)-1.25 \text{ Min}$

2x CLK Speed Operation:

$t_{SLDCL} \quad 2.25 \text{ Min}$

$t_{LCLKRWL} \quad 4.5 \text{ Min}$

$t_{DLDC} \quad 2.25 \text{ Max}$

$t_{HLDCH} \quad -2.0 \text{ Min}$

$t_{LCLKTWL} \quad (t_{CK}/4)-1 \text{ Min}, (t_{CK}/4)+1 \text{ Max}$

$t_{LCLKTWH} \quad (t_{CK}/4)-1 \text{ Min}, (t_{CK}/4)+1 \text{ Max}$

Calculation for maximum skew allowed between LCLK and LDATA at receiver:

At $t_{CK} = 25\text{ns}$

Setup Skew $2x = t_{LCLKTWH} (\text{Min}) - t_{DLDC} - t_{SLDCL} = (t_{CK}/4)-1 - 2.25 - 2.25 = 0.75 \text{ ns}$

Hold Skew $2x = t_{LCLKTWL} (\text{Min}) + t_{HLDCH} - t_{HLDCL} = (t_{CK}/4)-1 - 2 - 2.25 = 1 \text{ ns}$

Setup Skew $1x = t_{LCLKTWH} (\text{Min}) - t_{DLDC} - t_{SLDCL} = (t_{CK}/2)-1.25 - 2.5 - 3 = 5.75 \text{ ns}$

Hold Skew $1x = t_{LCLKTWL} (\text{Min}) + t_{HLDCH} - t_{HLDCL} = (t_{CK}/2)-1 - 3 - 3 = 5.5 \text{ ns}$

At $t_{CK} = 30\text{ns}$

Setup Skew $2x = t_{LCLKTWH} (\text{Min}) - t_{DLDC} - t_{SLDCL} = (t_{CK}/4)-1 - 2.25 - 2.25 = 2 \text{ ns}$

Hold Skew $2x = t_{LCLKTWL} (\text{Min}) + t_{HLDCH} - t_{HLDCL} = (t_{CK}/4)-1.25 - 1.75 - 2.25 = 2.25 \text{ ns}$

Setup Skew $1x = t_{LCLKTWH} (\text{Min}) - t_{DLDC} - t_{SLDCL} = (t_{CK}/2)-1.25 - 2.5 - 3 = 9.5 \text{ ns}$

Hold Skew $1x = t_{LCLKTWL} (\text{Min}) + t_{HLDCH} - t_{HLDCL} = (t_{CK}/2)-1 - 3 - 3 = 8 \text{ ns}$

Calculation for maximum transmission delay between two Link Ports:

- The maximum transmission delay (t_{PROP}) only is affected by the time required for the receiver to bring the LACK~ pin low at the transmitter if a stall is needed. LACK~ can be brought high asynchronous to the transmitter so t_{PROP} for that situation is not important.

- If a stall is required LACK~ is brought low by the receiver t_{DLALC} after the 2nd rising edge of LCLK~ at the receiver. LACK~ must be setup t_{SLACH} before the 8th (or 12th for 48-bit xfers) rising edge of LCLK at the transmitter.

- The transmission delay must satisfy this equation where t_{PROP} is the one way transmission delay of LACK~ pin:

$$(7*t_{CK}/2) \geq t_{DLALC} + t_{PROP} + t_{SLACH} + t_{PROP}$$

$$t_{PROP} \leq [(7*t_{CK}/2) - t_{DLALC} - t_{SLACH}]/2$$

At $t_{CK} = 25\text{ns}$

$$2x \text{ rate } t_{PROP} \leq [(7*t_{CK}/2) - t_{DLALC} - t_{SLACH}]/2 = [87.5-16-19]/2 = 26.25\text{ns}$$

$$1x \text{ rate } t_{PROP} \leq [(7*t_{CK}) - t_{DLALC} - t_{SLACH}]/2 = [175-16-19]/2 = 70\text{ns}$$

At $t_{CK} = 30\text{ns}$

$$2x \text{ rate } t_{PROP} \leq [(7*t_{CK}/2) - t_{DLALC} - t_{SLACH}]/2 = [105-16-19]/2 = 35\text{ns}$$

$$1x \text{ rate } t_{PROP} \leq [(7*t_{CK}) - t_{DLALC} - t_{SLACH}]/2 = [210-16-19]/2 = 87.5\text{ns}$$